**Amendments to the Claims:**

This listing of claims will replace all prior versions, and listing, of claims in the application.

**Listing of Claims:**

1. (Currently Amended) A thin film transistor array panel comprising:

an insulating substrate;

a gate wire formed on the insulating substrate and including a plurality of gate portions and a gate connection connecting the gate portions;

a data wire insulated from the gate wire and intersecting the gate[[data]] wire;

a gate insulating layer insulating the gate wire and the data wire, and including a plurality of portions, and a portion of the gate insulating layer is disposed between the plurality of gate portions and the gate connection;

a thin film transistor connected to the gate wire and the data wire; and

a pixel electrode connected to the thin film transistor.

2. (Original) The thin film transistor array panel of claim 1, wherein the data wire comprises a plurality of data portions and a data connection connecting the data portions.

3. (Cancelled)

4. (Original) The thin film transistor array panel of claim 1, further comprising a passivation layer covering the thin film transistors and including a plurality of portions.

5. (Currently Amended) The thin film transistor array panel of claim 2[[1]], wherein the gate connection is disposed on the same layer as the data portions, and connected to the gate portions through first contact holes provided at the gate insulating layer.

6. (Original) The thin film transistor array panel of claim 2, wherein the data connection is disposed on the same layer as the gate portions, and connected to the data portions through second contact holes provided at the gate insulating layer.

7. (Currently Amended) A thin film transistor array panel comprising:

an insulating substrate;

a gate wire formed on the insulating substrate;

a gate insulating layer formed on the gate wire and including first and second contact holes;

a semiconductor layer formed on a predetermined area of the gate insulating layer;

an ohmic contact layer formed on the semiconductor layer and having a shape substantially the same as the semiconductor layer except for a predetermined area of the semiconductor layer;

a data wire insulated from the gate wire, intersecting the gate wire, and overlapping the ohmic contact layer at least in part;

a passivation layer formed on the data wire and having a third contact hole exposing the data wire;

a pixel electrode formed on the passivation layer and connected to the data wire through the third contact hole,

wherein the gate wire includes first and second gate wire portions and a gate connection formed on the same layer as the data wire, a portion of the gate insulating layer is disposed between the first and second gate wire portions, and the gate connection, and the first and the second gate wire portions are connected to the gate connection through the first contact hole[[s]].

8. (Currently Amended) The thin film transistor array panel of claim 7, wherein the data wire includes first and second data wire portions and a data connection formed on the same layer as the gate wire, and the first and the second data wire portions are connected to the data connection through the second contact hole[[s]].

9. (Original) The thin film transistor array panel of claim 7, wherein the fist and the second gate wire portion comprises a gate line extending in a direction and a gate electrode, which is a portion of the gate line, and the first gate wire portion further comprises a gate pad provided at an end of the gate line.

10. (Original) The thin film transistor array panel of claim 7, wherein the gate wire and the data wire intersect to define a pixel area, and portions of at least one of the gate insulating layer and the passivation layer in the pixel electrode is removed.

11. (Original) The thin film transistor array panel of claim 8, wherein the first and the second data wire portion comprise a data line extending in a direction, a source electrode, which is a portion of the data line and overlaps the ohmic contact layer in part, and a drain electrode located opposite the source electrode and overlapping the ohmic contact layer in part, and the first data wire portion further comprises a data pad provided at an end of the data line.

12. (Original) The thin film transistor array panel of claim 10, wherein at least one of the gate insulating layer and the passivation layer is divided into a plurality of portions by an opening extending parallel to the gate wire, and the opening is located between adjacent gate lines and connected to the predetermined area of the pixel area.

13. (Withdrawn-Currently Amended) A method of manufacturing a thin film transistor array panel, the method comprising:

forming first and second gate wire and a data connection on an insulating substrate;

forming a gate insulating layer on the substrate;

forming a semiconductor layer and an ohmic contact layer pattern on the insulating layer partly overlapping the gate wire;

forming first and second contact holes in the gate insulating layer;

forming a gate connection connected to the first and the second gate wires through the first contact holes and first and second data wires partly overlapping the ohmic contact layer pattern connected to the data connection through the second contact holes on the substrate;

forming an ohmic contact layer by etching the ohmic contact layer pattern by using the data wire as a mask;

forming a passivation layer having a third contact hole on the substrate; and

forming a pixel electrode connected to the data wire through the third contact hole on the passivation layer.

14. (Withdrawn-Currently Amended) The method of claim 13[[14]], wherein the formation of the first and second contact holes includes formation of an opening for separating the gate insulating layer in the gate insulating layer.

15. (Withdrawn) The method of claim 13, wherein the formation of the passivation layer includes formation of an opening for separating the passivation layer in the passivation layer.